A Monolithic V-Band Upconverter Using 0.2 μm InGaAs/GaAs Pseudomorphic HEMT Technology

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ABSTRACT

A monolithic approach to V-band upconverter development has the advantages of lighter weight and lower cost over conventional hybrid approachs for high volume insertions into transmitter systems. This paper will present the design and performance of a complete monolithic upconverter macrocell using 0.2 μm InGaAs/GaAs pseudomorphic HEMT technology. Individual components, including a 2-10 GHz IF amplifier, a V-band upconverting mixer and a V-band amplifier are also described. The measured results demonstrate a conversion gain of 10 dB at V-band by injecting a 2-10 GHz IF frequency with an LO drive of 10 dBm at 54 GHz. This is the first reported monolithic upconverter with good performance and bandwidth at this frequency.

INTRODUCTION

The upconverter is an important component in the transmitting chain of a satellite communication system. This development uses high electron mobility transistors (HEMTs), which have demonstrated high gain and low noise capability at millimeter-wave frequencies. Several V-band monolithic low noise amplifiers (LNAs) using HEMT technology have been previously reported [1]-[3], while a V-band diode mixer using a MESFET compatible process was reported in [4]. Recent refinements in HEMT modeling and process technology make it possible to realize a high level of integration for monolithic millimeter-wave IC's, especially for the V-band amplifier and mixer.

The monolithic upconverter demonstrates a conversion gain of 10 dB when converting a 2-10 GHz IF signal to V-band with an LO drive of +10 dBm at 54 GHz. The individual components were also fabricated on the same wafer and tested. A rigorous design/analysis methodology was utilized in the monolithic chip development, which includes accurate device modeling and full-wave electromagnetic (EM) analysis of passive structures [6]. The success of this chip development is attributed to the stable HEMT processing technology and the rigorous design methodology. To our knowledge, this is the first reported monolithic upconverter at this frequency.

MONOLITHIC UPCONVERTER AND INDIVIDUAL COMPONENTS

Fig. 1. shows the block diagram of the recently developed monolithic upconverter, which includes a 2-10 GHz IF HEMT LNA, a V-band HEMT diode mixer, and a two-stage 60 GHz output amplifier.

The monolithic circuits are fabricated on a 3 inch diameter GaAs wafer thinned down to 100 μm using 0.2 μm T-gate pseudomorphic (PM) HEMTs. The analysis procedures incorporated in this MMIC design are similar to the W-band

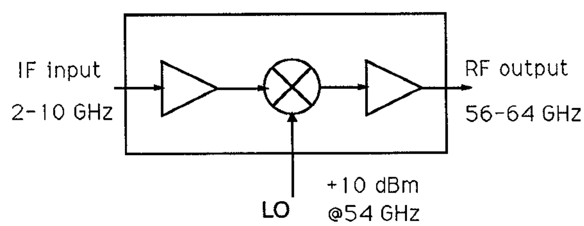

Fig. 1. Block digram of the V-band monolithic upconverter.

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monolithic LNA design reported in [5]. The HEMT device linear model was obtained by fitting measured S-parameters to 40 GHz and noise model generated by measured noise parameters to 26 GHz. DC $I-V$ curves were used for the device nonlinear characterization. Both linear and non-linear circuit simulations were performed during the design to predict the circuit performance. The individual circuit designs are described as follows.

V-band Output Amplifer

The V-band output amplifier is a two-stage single-ended design similar to the one reported earlier [2]. The circuit schematic diagram and photograph of the chip are shown in Fig. 2. Each stage utilized a 40 μm gate width HEMT with 4 gate fingers. The matching circuits comprised of series transmission lines open stubs, and metal-insulator-metal (MIM) capacitors. The radial stubs and shunt MIM capacitors were used as RF ground at gate and drain bias networks, respectively. The interstage DC block was realized by MIM capacitors. The on-chip bias networks were carefully designed for unconditional stability. The chip size is 3.6 × 2.0 mm^2.

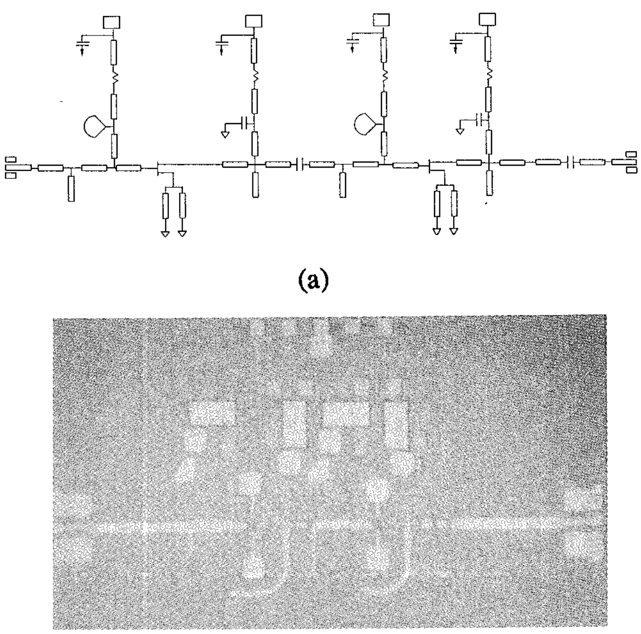


Fig. 2. (a) Circuit schematic diagram and (b) chip photograph of the monolithic V-band LNA.

Singly Balanced Diode Mixer

The frequency upconverting mixer is a singly balanced design using two diodes. Fig. 3 illustrates the circuit schematic diagram and chip photograph. The chip size is 3.6 × 2.0 mm^2. It converts a 2-10 GHz IF signal to 56-64 GHz RF signal using an LO frequency at 54 GHz. The Schottky gate diode is realized by connecting the drain and source terminals of a HEMT as the anode. The modified rat-race which consists of a Lange coupler and a three-quarter wavelength microstrip line is chosen as the balun. This balun provides 180^o phase shift for 3 dB power splitting in a wide bandwidth so that the mixer can be used as either a broad band frequency upconverter or downconverter [7].

Distributed IF Amplifier

The 2-10 GHz IF amplifier utilizes a 5-cell distributed architecture to achieve wide bandwidth. The design is similar to the one reported in [8]. Both 90 μm and 120 μm PM

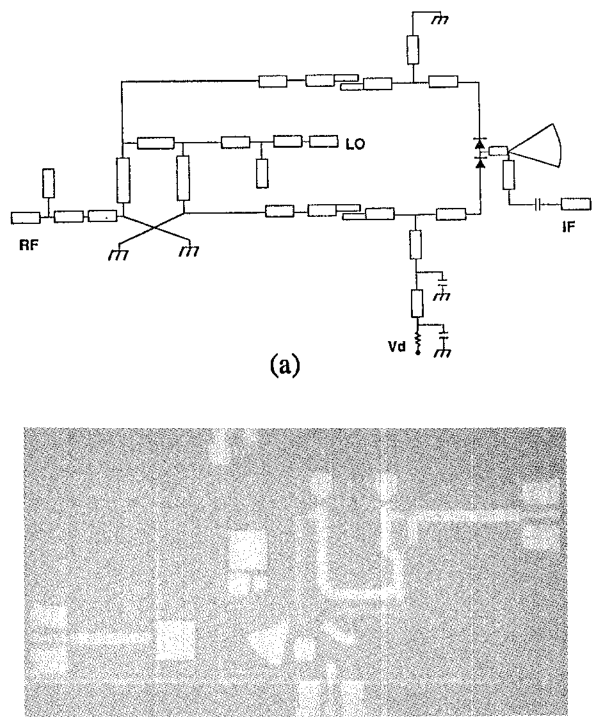


Fig. 3. (a) Circuit schematic diagram and (b) chip photograph of the monolithic singly balanced diode mixer.

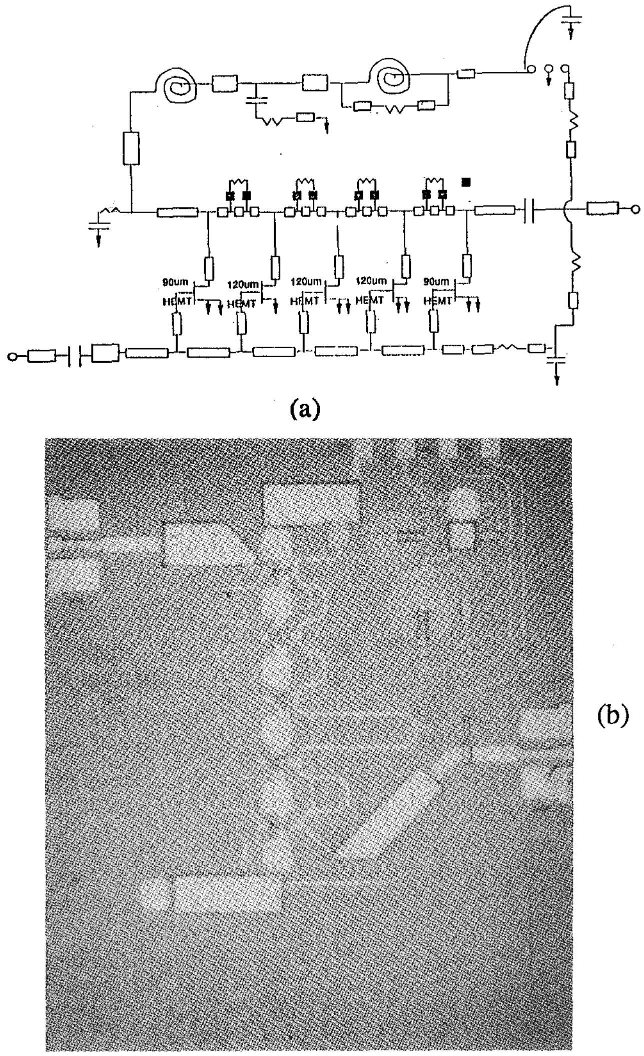
HEMTs are used in the design. The distributed amplifier was optimized for broad band low noise performance. The circuit schematic diagram and chip photograph are shown in Fig. 4. The chip size is 2.6 × 3.0 mm^2.

Upconverter Design

The upconverter is realized by cascading the IF amplifier as the front end, followed by the upconverting mixer. The mixer output is connected to input of the V-band output amplifier. Since each component is matched to 50 Ω environment, 50 Ω transmission lines are used to join the circuits. A photograph of the monolithic upconverter is shown in Fig. 5. The chip size is 9.6 × 3.0 mm^2.

MEASURED PERFORMANCE

On-wafer RF probing technique was used to measure all MMICs. The V-band output amplifier has a measured gain of 8 dB and input VSWR better than 2.3 from 54 GHz to 60 GHz as shown in Fig. 6(a). The IF amplifier demonstrates a gain of 10 dB with input and output VSWR better than 1.8 from 2 to 10 GHz as indicated in Fig. 6(b). The upconverting mixer shows a measured conversion loss of 8 dB when injecting an IF signal of 2-10 GHz with an LO drive of +10 dBm at 54 GHz with 1.2 V bias voltage. The complete upconverter measurement results are shown in Fig. 6(c). It demonstrates 10 dB conversion gain with a IF signal of -30 dBm at 2-10 GHz and an LO drive of +10 dBm at 54 GHz.



(a)

(b)

Fig. 4. (a) Circuit schematic diagram and (b) chip photograph of the monolithic distributed IF amplifier.

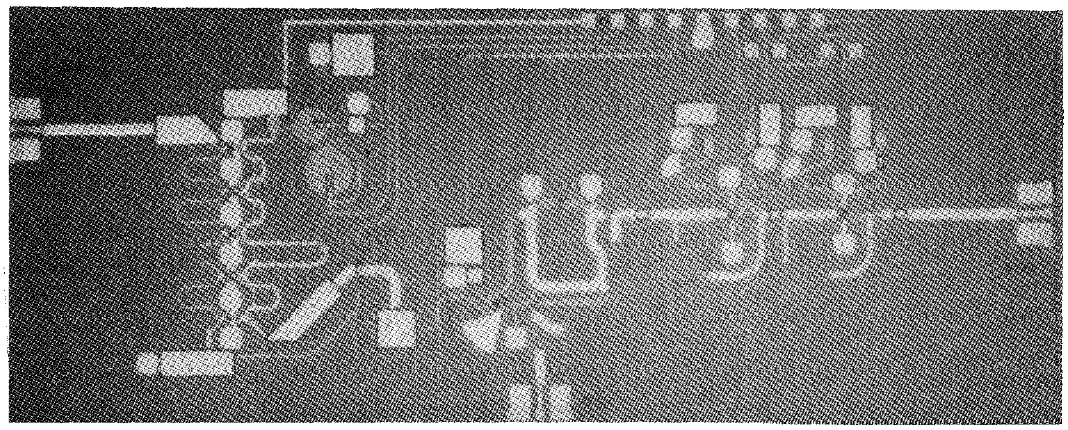


Fig. 5. Chip photograph of the monolithic upconverter.

SUMMARY

We have presented the recent development of a V-band monolithic upconverter using 0.2 μm pseudomorphic HEMT technology. The monolithic upconverter demonstrates a measured conversion gain of 10 dB at 2-10 GHz IF frequency with an LO drive of +10 dBm at 54 GHz. These results represent state-of-the-art performance of high-level integration of MMICs at this frequency and make this monolithic upconverter chip ideal for satellite communication link applications. The stable MMIC processing technology and rigorous design/analysis methodology are the foundations of this successful V-band monolithic IC development.

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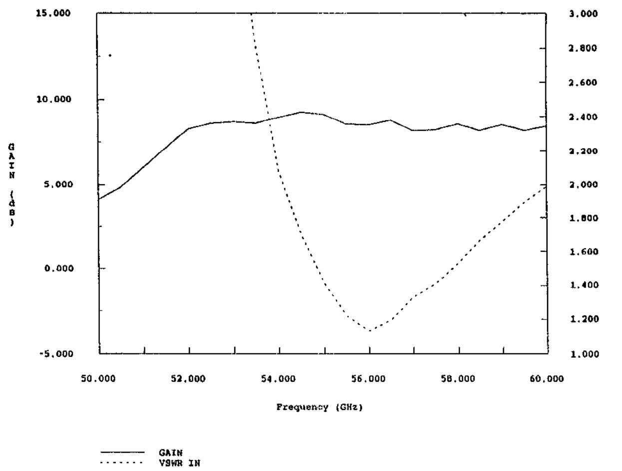
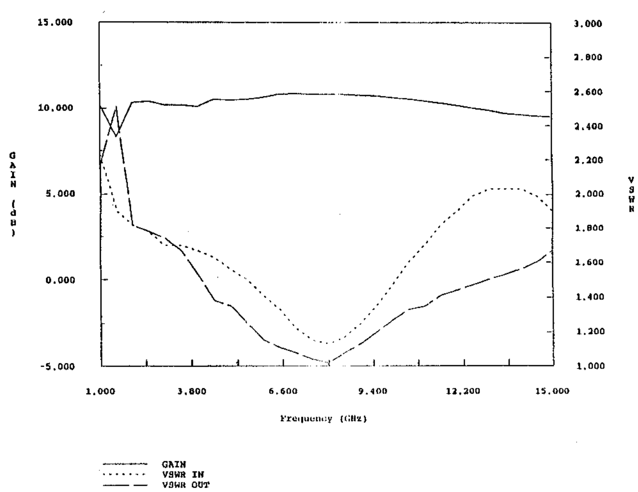
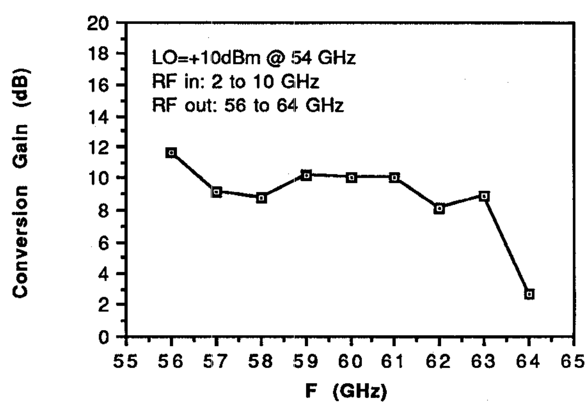


(a)



(b)



(c)

Fig. 6. Measurement results of (a) V-band amplifier, (b) distributed IF amplifier and (c) monolithic upconverter.